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ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 06/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/669,762	HUSHER, JOHN DURBIN	
	Examiner	Art Unit	
	Lex Malsawma	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Sep. 24, 2003 through Nov. 03, 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/3/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Abstract

1. Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is **a concise statement of the technical disclosure** of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

The abstract should be in narrative form and **generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words**. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

2. The abstract of the disclosure is objected to because it does not contain a concise statement of the process steps relevant to the current invention, i.e., the examiner suggests shortening the abstract to one paragraph highlighting process steps relevant to the inventive aspect of the current disclosure. Correction is required. See MPEP § 608.01(b).

Specification

3. The disclosure is objected to because of the following informalities:

On page 4 (line 2) of the current specification, it seems reference characters "202" and "700" should be changed to "502" and "500", respectively;

the current specification does not include descriptions specifically related to the reference numerals shown in the drawings (for example, note the reference characters shown in Figs. 2A-2G);

the current specification refers to figures the do not exist in the current drawings, for example, note on page 10 (in lines 2-4), figures 4A and 4B are referenced, and on page 13 (last paragraph), figures 10A and 10B are referenced; and

the current application is a continuation of U.S. Pat. Application Ser. No. 10/034,184; however, the current specification and drawings are significantly different from the specification and drawings in Application Ser. No. 10/034,184. For example, compare the section titled, "SUMMARY OF THE INVENTION", with the equivalent section in Application 10/034,184, and also compare figures 2d in both applications. Please note that these two specific examples are only a portion of the numerous differences between the two applications. It seems that the current application may qualify as a continuation-in-part (CIP) application; however, if the applicant maintains that the current application is a continuation application and not a CIP application, then a marked-up version of the current specification showing the changes must be provided along with a statement that no new matter has been added. Please note the portion of MPEP § 201.07 reproduced hereinafter. Appropriate correction is required.

201.07 [R-2] Continuation Application

A continuation is a second application for the same invention claimed in a prior nonprovisional application and filed before the original prior application becomes abandoned or patented. The continuation application may be filed under 37 CFR 1.53(b) >(<or 1.53(d) >if the application is a design application)<. The applicant in the continuation application must include at least one inventor named in the prior nonprovisional application. **The disclosure presented in the continuation must be the same as that of the original application; i.e., the continuation should not include anything which would constitute new matter if inserted in the original application**. The continuation application must claim the benefit of the prior nonprovisional application under 35 U.S.C. 120 or 365(c).

Drawings

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include numerous reference character(s) not mentioned in the description: For example, none of the reference numerals in figures 2A-2G are mentioned in the specification. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New

Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1:

This claim contains numerous limitations for which there are insufficient antecedent basis. More specifically, the following limitations lack antecedent basis:

in line 7, "the remaining silicon";

in lines 8-9, "the location of the buried power buss (BPB)";

in lines 10-11, "the buried metal";

in line 13, "the top surface", i.e., the top surface of what?;

in line 15, "the power buss (PB)"; and

in line 16, "the final metal deposition".

Furthermore, it is not clear if the "triple metal technology" is provided in conjunction with processing a single metal and patterning a single thin metal, where the single metal and the single thin metal are one of the three metal layers or one of the three metal levels (note lines 11-

12), wherein each of the metal levels can consist of a plurality of layers (as the one buried layer consisting of two layers, in line 14). In other words, it seems the triple metal technology comprises a plurality of processes including steps for forming at least three metal layers; accordingly, it is not clear *whether the limitation*, "all while providing single metal processing and patterning of a single thin metal", *refers to* a process for forming one of the metal layers "within" the triple metal technology" *or* to a process for forming a single thin metal in some other region of the substrate.

In sum, claim 1 is indefinite primarily because it does not recite a coherent process in which the process steps have a logical order or sequence.

Regarding claim 4:

"the high temperature" and "the junction isolation" lack antecedent basis.

Regarding claim 5:

"the high temperature" and "the sinker" lack antecedent basis.

Regarding claim 7:

"the sinker" lack antecedent basis. Furthermore, this claim requires opening slots in the dielectric layer prior to metal to allow removal of the oxide formed by oxidizing the slots; however, in claim 1, the dielectric is coated over the slots "after" providing metal in the slots, wherein the metal is provided "after" forming the oxide, i.e., there would be metal sandwiched between the dielectric and the oxide. Therefore, it is not clear how slots can be opened in the dielectric prior to metal, especially because claim 1 requires the dielectric to be coated over the slots. Accordingly, this claim cannot be properly examined.

Regarding claims 8 and 11:

In each claim, the examiner suggests deleting "versus junction isolation" because such a comparison is not relevant to the patentability of the claim, especially because no definitive means/measure has been disclosed for comparing oxide isolation and junction isolation.

Regarding claim 9:

In line 1, after "claim 1", "wherein" should be inserted.

Regarding claim 10:

In lines 1 and 3, "the design critical dimensions" and "the technologies" lack antecedent basis; and in line 2, the recitation, "can be significantly reduced and in many cases can touch", renders this claim indefinite because it is not clear as to "how far from touching" would be considered to be "significantly reduced".

Regarding claims 12-14:

"the various technologies" lack antecedent basis.

Regarding claim 15:

This claim is indefinite because it seems to require the three layers of metal to have an "insulating layer" positioned/sandwiched between each of the three metal layers, wherein the there metal layer are positioned one on top of another (note claim 1, lines 13-15); however, if this be the case, then the power buss (PB) would not be properly connected (electrically) to the contacts. Furthermore, it is not clear whether "a single thin layer (the last deposited)" refers to "the final metal deposition" (in claim 1) or to any thin layer that is last deposited, whether the thin layer is a metal or a dielectric.

Regarding claim 16:

The examiner suggests deleting the entire phrase, ", versus standard triple metal processes...(or via) etched" because such a comparison is not relevant to the patentability of the claim, especially since the instant claim does not recite "an improvement" over the standard process.

Regarding claim 18:

Claim 1 does not mention "high current" or "thick metal"; therefore, "the high current" and "thick metals" lack antecedent basis. Furthermore, in line 2, "the third layer" lacks antecedent basis.

Regarding claims 2, 3, 6, 8, 11, 17 and 19:

These claims are indefinite because they depend from an indefinite claim (claim 1).

Any further rejections of, or indication of the allowability of, claims 1-19 are based on the claims are they are understood/interpreted by the examiner.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-6, 8 and 10-19 (all as best understood) are rejected under 35 U.S.C. 103(a) as being unpatentable over **Rhodes** (US 2005/0074966 A1) in view of Choi et al. (5,629,238; hereinafter "**Choi**").

Regarding claim 1:

Rhodes discloses a method of providing an improved integrated circuit device comprising the steps of:

providing active and passive areas in a substrate (200/202/209, i.e., note Fig. 2, the substrate being referenced is a combination of regions 200, 202 and 209; and note in paragraph 0017, region 200 comprises active areas such as NWELLs, PWELLs, etc., and regions 202 and 209 are a passive areas, i.e., these regions are formed of electrically insulative material);

providing a plurality of slots (215, 218, 221, Fig. 2 and paragraph 0018) in the substrate after providing the active and passive areas;

providing metal (224, 227) in each of the plurality of slots and providing a dielectric coating 309 over the slots and the remaining portion of the substrate (Figs. 2, 5 and paragraphs 0029 and 0037);

providing an etched contact in a select area (i.e., within slot 218) remote for the location of a buried electrical interconnect (within slot 215, note Fig. 5 and paragraph 0022, wherein Rhodes discloses the conductive materials within the slots are capable of functioning as electrical interconnects, accordingly, the interconnect defined by slot "215" could obviously be referred to as a buried power buss "BPB");

providing an additional layer of metal 230 that interconnects the contact and buried metal (224, 227) in select areas (within slot 218) where contacts were opened, thereby providing an electrical interconnect capable of functioning as a power buss (PB) and resulting in metal of three levels (224, 227, 230); and

providing triple metal technology with one layer 230 on the top surface of another layer 227, one layer that is buried consisting of two layers of metal (224 and 227) buried in slot 215 (note Fig. 5) capable of functioning as a buried power buss (BPB), and the power buss (PB) that has three layers of metal (224, 227, 230) located where a contact was opened (in slot 218) prior to deposition of a final metal 230; all while providing single metal processing and patterning of a single thin metal wire-bond 403 (Fig. 5), i.e., when gold wire 403 is wire-bonded, it is processed such that the thin gold wire has a "bonded" semi-spherical pattern with a wire extending therefrom.

Rhodes **lacks** oxidizing the plurality of slots. Choi **teaches** a process for forming conductive lines within slots formed in a low-dielectric-constant insulating layer 16 comprising a fluorinated silicon oxide, SiOF, (note Figs. 6A-6C), wherein the process includes oxidizing the slots, i.e., after the slots are formed in SiOF layer 16, a silicon dioxide layer is formed on surfaces of the slots (note Fig. 6A and Col. 3, line 66 to Col. 4, line 1). Choi teaches that such a process prevents deterioration of the SiOF layer (note Col. 3, lines 16-21). It would have been obvious to one of ordinary skill in the art to modify Rhodes by oxidizing the plurality of slots (as taught by Choi) because an oxide formed on the slot surfaces would prevent deterioration of the insulating layer 209, especially in a case where the insulating layer 209 is a fluorinated silicon oxide such as SiOF (note that Rhodes discloses fluorinated-silicon-oxide as a suitable material for insulating layer 209, see Rhodes, paragraph 0021).

Regarding claim 2:

Rhodes discloses insulating layer 209 is an oxide (paragraph 0021); therefore, the triple metal technology (in Rhodes) provides three independent oxide-isolated metal layers (in slots

215, 218 and 221) being of sufficient thickness to carry high current. Note that "high" is a relative term; accordingly any current carried by the oxide-isolated metal layers could be specified as "high current". Therefore, this claim is held obvious over the cited references.

Regarding claim 3:

Rhodes discloses the slots (215, 218, 221) are placed in a single insulating layer 209; therefore, the slots are placed in a manner that minimizes the process steps for manufacture.

Regarding claims 4 and 5:

Rhodes does not mention "junction isolation" or a "sinker", therefore, high temperature and long time process for forming a "junction isolation" or a "sinker" are eliminated.

Regarding claim 6:

Rhodes discloses (in paragraph 0017) the substrate region 200 comprises regions including NWELLs, PWELLs, transistor implants and source-drain implants, where these regions are essential parts of bipolar, CMOS, BICMOS, DMOS and/or BCD technologies. Given Rhodes (in view of Choi), it would have been obvious one of ordinary skill in the art to recite that the active and passive areas are provided for bipolar, CMOS, BICMOS, DMOS and/or BCD technologies with improved properties because such a recitation could be generally made for any metallization process related to said technologies. In other words, no quantifiable measure of improvement has been claimed or disclosed in the current disclosure; therefore, the limitation in the instant claim is considered to be a generalized statement, which could be readily attributed to Rhodes (in view of Choi).

Regarding claim 10:

Rhodes discloses the passive area "202" is in contact with region "200" of the substrate, wherein region "200" comprises active areas such as NWELLs, PWELLs, etc.; therefore, design critical dimensions between active areas and passive areas are significantly reduced because the active (200) and passive (202) areas touch (note Figs. 2, 5 and paragraph 0017); accordingly, Rhodes provides a significant reduction in die size of a "technology".

Regarding claims 8 and 11:

Rhodes discloses the insulating layer 209 comprises oxide (paragraph 0021); therefore, oxide isolation is provided, accordingly, coupling capacitances are greatly reduced versus junction isolation. Note that, "greatly reduced", is relative terminology and a "coupling capacitance" for the claimed oxide isolation has not been quantified; accordingly, any measured coupling-capacitance could be referred to as being greatly reduced in comparison to that for a junction isolation, especially where a coupling-capacitance for the "junction isolation" has also not been quantified by any suitable, measurable or comparable means.

Regarding claims 12-14:

These claims contain general statements that could be readily attributed to any process, in the relevant art, for forming conductive interconnects within slots/trenches. Therefore, Rhodes discloses slots that are ideally located to provide significant parametric, circuit and system advantages for various technologies.

Regarding claim 15:

Rhodes discloses three layers of thick metal (224, 227, 230) of three different thicknesses, each isolated laterally from one another, while only requiring to etch a single thin

layer 309, which is the last deposited layer (Fig. 5 and paragraph 0037), i.e., as shown in Fig. 5, passivation/dielectric layer "309" is thin in comparison to dielectric layer "209". Note that "thick" is a relative term, therefore, the three layers of metal (224, 227, 230) are considered to be "thick" (50-1000 angstroms for "224", 100-1000 angstroms for "227', and in Fig. 5, layer "230" is shown to be considerably thicker that either layer "224" or "227").

Regarding claim 16:

Choi discloses only one layer of dielectric 22 needs to be deposited and contact etched (prior to depositing metal into the slots, note Figs. 6A-6B). Therefore, Rhodes, modified as taught by Choi, discloses three layers (224, 227, 230) of isolated metal interconnect are formed while only requiring one layer of dielectric to be deposited and contact etched.

Regarding claim 17:

Initially, note that, "very thick", is relative terminology. Therefore, Rhodes discloses two very thick layers of metal (227, 230) in the BPB (defined by slot 215 in Fig. 5) and three layers of metal (224, 227, 230) in the PB (defined by slot 218 in Fig. 5) and a single layer of metal 403 on the top surface without metal "403" having to cross over high metal steps (i.e., without having to cross over any metal steps, since layer "309" is a dielectric). Note that metal layer 227, having a thickness range from 100-1000 angstroms, is very thick relative to a monolayer of copper; accordingly, layers "227" and "230" can be referred to as being very thick layers of metal.

Regarding claim 18:

Rhodes discloses (in paragraph 0022) the conductive lines/interconnects are capable of functioning as electrical interconnects for integrated circuits; therefore, high current would be

carried on the BPB and PB with their metals (227, 230), which are relatively thick metals in comparison to a monolayer of copper, and a third layer 303 (Fig. 3) capable of interconnecting low power circuitry (note lines 5-7 in paragraph 0022).

Regarding claim 19:

The limitations within this claim are not considered to carry any patentable weight because they refer to features for specific devices such are CMOS, BICMOS, etc., but the process recited in claim 1 is directed to forming conductive lines/interconnects within slots. In other words, no specific process steps for forming the "specified devices" have been disclosed/claimed, and the current specification does not include a detailed description of how the "conductive lines/interconnects" are incorporated within the "specified devices"; therefore, the "improved parameters" recited in the instant claim are considered to be general statements readily attributable to Rhodes' conductive lines/interconnects. In other words, there is nothing in Rhodes (or Choi) to prevent one from reciting the claimed "improved parameters" in conjunction with Rhodes' conductive lines/interconnects. Therefore, this claim is held obvious over Rhodes (in view of Choi).

9. Claim 9 (as best understood) is rejected under 35 U.S.C. 103(a) as being unpatentable over **Rhodes** (in view of **Choi**) as applied to claim 1 above, and further in view of Sahara et al (4,764,804; hereinafter "**Sahara**") and Lin et al. (5,450,283; hereinafter "**Lin**").

Regarding claim 9:

Rhodes (in view of Choi) **lacks** only one layer of metal requiring masking and pattern etching; however, note that Rhodes utilizes a wire-bond 403 as an attaching means. Sahara and

Lin are cited primarily to show that it was well known in the art that "flip-chip bonding" has advantages over wire bonding. Lin **teaches** that an advantage of using flip-chip bonding is that wire-bonds are eliminated such that protecting the wire bonds and their respective wire loops is not required (Col. 3, lines 50-56). However, Lin does not provide details regarding the attaching means in a typical flip-chip bond. Sahara is **cited only to show** that a flip-chip bond typically includes a thin metal layer 10 (Fig. 2) formed/patterned such that it connects to a conductive layer 7 located within a recess provided by a dielectric layer 11. Note the recess formed in dielectric layer 11 (of Sahara) is similar to the recess formed in the Rhodes' dielectric layer 309 (Fig. 5). It would have been obvious to one of ordinary skill in the art to modify Rhodes (in view of Choi) by replacing the wire-bond with a flip-chip bond because Lin teaches that such a modification would eliminate the need for protecting the wire bond and wire loop, and when the wire-bond (in Rhodes) is replaced with a flip-chip bond, Sahara shows that only one layer of metal would require masking and pattern etching. Therefore, Rhodes (in view of Choi, Lin and Sahara) discloses three layers of metal (224, 227, 230, for the conductive lines/interconnects) with only one layer of metal for the flip-chip bond, which requires masking and pattern etching.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The references listed on the attached Form PTO-892 (not cited above) are cited to show processes for forming interconnect wiring within slots using multiple metal layers, dielectric liners, sinker-replacement contacts, etc.

Note that U.S. Pat. Nos. 6,894,393 B1 and 6,882,053 B1 are the patents of the two U.S. Pat. Application Ser. Nos. 10/034,067 and 10/034,279 (respectively) that were indicated to be related applications within the specification of U.S. Pat. Application Ser. No. 10/034,184, which is the parent of the current application.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lex Malsawma whose telephone number is 571-272-1903. The examiner can normally be reached on Mon. - Thur. (4-12 hours between 5:30AM and 10 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lex Malsawma

June 15, 2005